



SHORT COURSE ON

Modeling and Simulation of Nano-Transistors

JANUARY 21 - 25, 2019

Organized by Department of Electrical Engineering, IIT Kanpur



Website

<http://www.iitk.ac.in/nanolab/sc2019>

Registration Form

<http://www.iitk.ac.in/nanolab/sc2019>

Registration Fee **

Industry/R&D Labs: Rs. 15,000

Faculty: Rs. 9,000

Students: Rs. 6,000

Coordinators

Dr. Y. S. Chauhan, IIT Kanpur

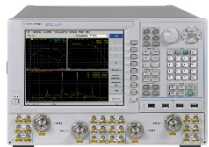
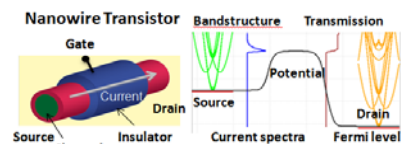
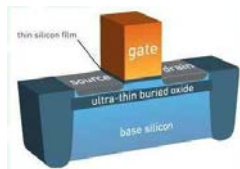
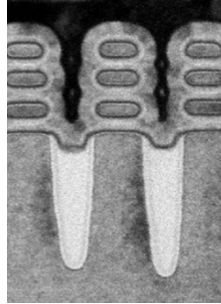
Dr. A. Agarwal, IIT Kanpur

Contact

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Topics:

- VLSI design and Nanoelectronics
- Physics and Operation of MOSFET
- SPICE and Circuit simulation
- TCAD simulation: Theory and demonstration
- Compact Modeling: Theory and demonstration
- Scaling and Moore's Law
- Nano-Transistors: FinFET, FDSOI, Negative Capacitance FET
- Nanosheet FETs, 2D-FETs etc.
- Characterization: Current and capacitance measurement
- RF CMOS and GaN High Electron Mobility Transistors



Also included:

- Laboratory visits and RF transistor measurement
- New research problems in Nanoelectronics
- How to write research project and papers

Target Audience:

Faculty members, practicing engineers & students.

SPEAKERS



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**Registration Fee includes course fee, accommodation, meals, printed lecture notes and stationery.