Basics of CMOS Device Technology and Optical Lithography

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Objective: In this tutorial, we will cover basics of MOSFET device design, highlighting the process contribution to making an advanced MOSFET. Challenges faced in device scaling at 32-nm node and beyond will be discussed, followed by the recent advances in MOSFET architectures such as the double gate and FinFETs. In order to realize these devices on Silicon, optical lithography is used to print designs much beyond the classical resolution limit of the imaging system. The resolution enhancement techniques are essentially computational in nature encompassing optical imaging, optimization theory and efficient computation. In this tutorial, the basics of lithography imaging theory and efficient numerical formulations for image calculations will be presented. The optimization techniques that are used to device predictive resist development models will also be discussed. Finally we will describe some of the promising resolution enhancement techniques for 22 nm and 14 nm technology development.

Speaker Bio:

Abhisek Dixit received the MTech degree from Indian Institute of Technology Bombay in 2002 and PhD in Electrical Engineering from Inter-university Microelectronics Center (IMEC) Belgium in 2007. His PhD thesis was on 32-nm SOI FinFET device design and process integration. He joined the IBM Semiconductor Research and Development Center (SRDC) in the compact modeling group, where he leads modeling projects for various value-added foundry technologies. His current research interests include device design, variability and CMOS processing of 14-nm SOI transistors.

Samit Barai received the PhD degree in Physics from IIT Delhi, New Delhi, India. He has earlier worked with KLA- Tencor Pvt. Ltd. and developed aberration monitoring models for high NA wafer inspection tools. He is presently leading process modeling team of the Semiconductor Research and Development Center (SRDC) of IBM at Bangalore. He is active in the development of lithography process and resolution enhancement techniques to enable 22nm node integrated circuits to the end user. His interests are in the area of computational lithography and computational methods for optical devices.